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Top down fabricated silicon nanowire networks for thermoelectric applications

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ABSTRACT

A top down process for the reliable fabrication of very complex, large area (order of millimeter square), nets of well organized and connected silicon nanowires (SiNWs) is shown and discussed. It will be shown that these nets are equivalent to the parallel of many very narrow, millimeter long, silicon nanowires, that can be employed either for the fabrication of high efficiency thermoelectric generators or for nanosensing devices.

The high reliability with respect to nanowire failure and the high tolerance with respect to silicon nanowire width dispersion are demonstrated by means of numerical simulations. Electrical measurements are reported and compared with numerical simulations, in order to confirm both the equivalence of the net to the parallel of millimeters long SiNWs and its high tolerance with respect to nanowire failure.

1. Introduction

Silicon nanowires (SiNWs) are very promising building blocks for the realization of innovative devices with important applications in many fields as sensing [1], nanoelectromechanical systems (NEMS) and other innovative electron devices [2]. In particular, as recently demonstrated [3,4], thermal conduction of very small SiNWs is drastically reduced with respect to bulk silicon. Thermal conductivities of the order of few W/mK have been theoretically predicted [5] and measured for SiNW with rough surfaces [4,6,7]. The reduced SiNW thermal conductivity gives interesting possibilities for the fabrication of devices to be used for thermoelectric generation with high heat to electrical power conversion efficiency. These devices could be usefully employed for energy harvesting purposes. However, for the development of usable SiNW based thermoelectric generators, a technique for a massive and reliable production of well organized, very long, SiNWs must be available. Such a technology could also be employed for the fabrication of sensing devices based on large arrays of very sensitive nanowires. The aim of the present work is to present a top down technique for the realization of a well organized and very reliable network based on a large amount (order of 10^5 SiNWs per mm^2) of narrow (<50 nm) silicon nanowires. In ideal conditions (i.e. no defects are present) these very large area SiNW arrays are equivalent to the parallel of many very long (order of millimeters) and small SiNWs. On the other hand, as it will be shown in the next sections, the arrays are much more tolerant to unavoidable random defects of single, very long, nanowires.

2. Nanowire network fabrication

Fig. 1 shows SEM photos of a typical top down fabricated SiNW net. On the left, a low magnification image of a $1 \times 0.6\ mm^2$ area SiNW network (dark zone of the image) is shown; clear areas are continuous silicon, and a trench (dark) runs at the borders of the net to provide electrical insulation. Conduction is measured (see the next sections) between crystalline silicon areas (top and bottom terminals) which are accessed through aluminum contacts (not visible). On the right, the texture of the net, made of SiNWs 3 μm long, is shown; the SEM image of the inset shows the 50 nm wide Si core, embedded in silicon dioxide. The implemented fabrication technique is an advancement of a previously developed top down process [8,9] that allows reliable fabrication of devices based on narrow (down to 10 nm), micrometers long, single SiNWs. The process is developed on Silicon On Insulator (SOI) substrates, with a top silicon layer 260 nm thick. Doping of the top silicon layer has been obtained by means of a solid source doping technique. The effective doping and carrier mobility of silicon nanowires are still an open problem, because they depend on many factors such as interfacial states density, surface segregation of doping species and so on. A silicon dioxide layer is grown on top by dry thermal oxidation. A suitable SiO_2 mask is then obtained by a high resolution electron beam lithography step [10], through standard PMMA resist and calibrated chemical wet etching. A procedure for the correction of electron beam lithography intra proximity effects has been developed in order to obtain a more uniform exposure on large areas. As shown in Fig. 2 the SiNW network is defined by writing several rows of boxes, starting from one corner of the structure that we want to fabricate. Moreover, the device is isolated from the whole Si chip by means of lateral trenches. The dose is partially compensated along the transverse writing

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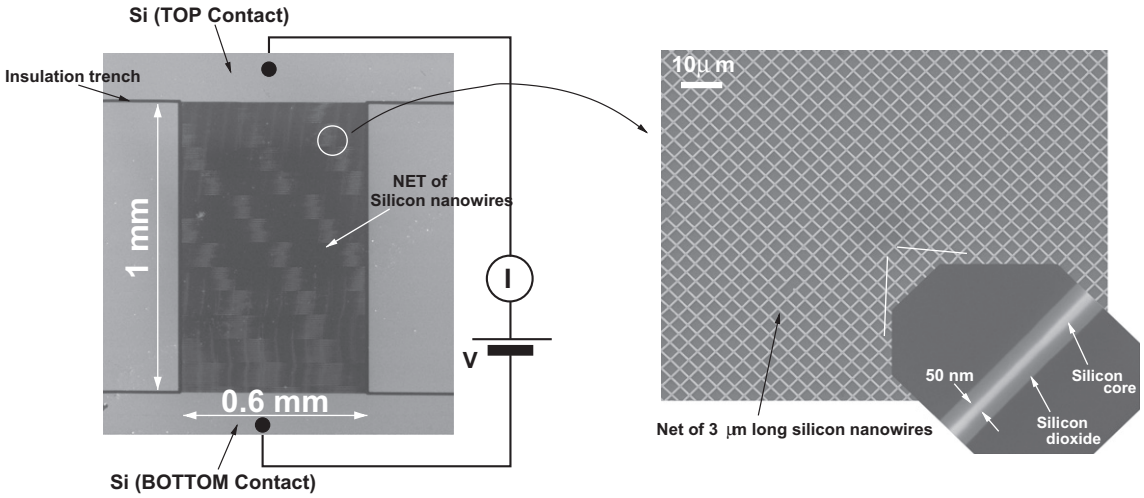

Fig. 1. SEM images of a silicon nanowire network. On the left, a low magnification image showing the overall dimension of the network. On the right, the texture made of 3 μm long SiNW is shown; the inset shows a detail of the SiNW with a core width of 50 nm.

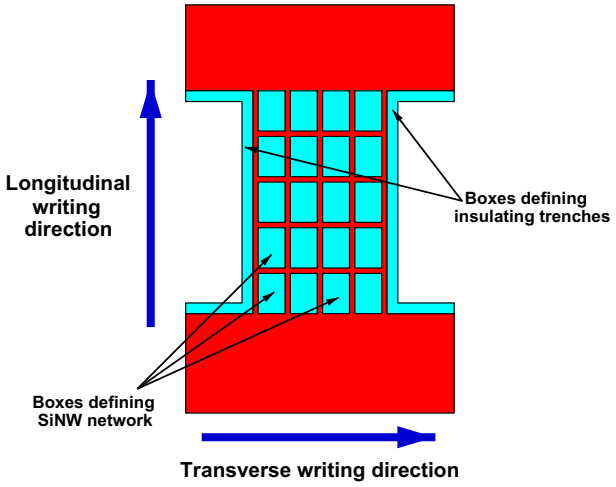

Fig. 2. A sketch of the adopted e-beam writing strategy and of the intra proximity effect correction. Lighter areas are exposed by e-beam.

direction by tuning the exposure dose of the insulating trenches. On the other hand, the compensation in the longitudinal writing direction is obtained by varying the exposure dose of each box, that is larger at the boundaries and it is reduced toward the center of the device. Silicon anisotropic wet etching has been used in order to obtain very uniform wires with trapezoidal cross section, laterally delimited by (1 1 1) silicon crystalline planes. Stress controlled oxidation [9] is then used for defining the SiNWs and reducing their width in a well controlled and reliable way. At the end of the oxidation process, each silicon nanowire has a triangular cross section. As it has been demonstrated [11], by using this technique it is possible to obtain very narrow SiNWs even starting by not very small initial structures (over 100–150 nm of initial width), that could be obtained even with advanced optical lithography, in order to reduce fabrication costs and extend the nanonet area. The initial width of the nanowires is limited only by the maximum nanowire density that has to be obtained in the final device.

3. Random failures in SiNW networks

As schematically represented in the sketches of Fig. 3a and 3b, a defectless silicon nanowire network is equivalent to many parallel silicon nanowires, each of the same width of the SiNWs forming the texture and of the same length of the whole net (1 mm in the case of the net shown in Fig. 1). In particular, important properties connected to the low nanowire width, such as large electrical to thermal conductivity ratio, are preserved; in Fig. 3c a sketch of the electrical equivalent resistor network is shown. Each of the $N \times M$ (row by column) resistors of the network models a SiNW of the net texture with a resistance value R_0 (conductance value $G_0 = 1/R_0$). Using symmetry arguments, it is trivial to demonstrate that this resistor network is equivalent to M parallel resistors, each given by the series of N elementary resistor of the network that are the vertical branches in the sketch of Fig. 3c. In the case of a perfect network, horizontal branches are ineffective both for the electrical and for the thermal conduction. The key point in using a silicon nanowire network, instead of parallel long wires, is that this structure is much more tolerant to nanowire failures (e.g. breaking) that can occur during the fabrication process for the presence of defects. This allows the fabrication of very large areas SiNW networks (equivalent to millimeters long SiNWs in parallel) with high reliability and repeatability of the total thermal and electrical resistance of the net.

In order to give a quantitative support to these considerations, a Monte Carlo technique has been implemented and applied to resistor networks. An ad hoc program for the resolution of electrical networks with a great number of resistances, based on a recursive optimized $Y - \Delta$ transformations [12], has been developed in order to optimize computational time. The program has been tested on a complete network of $N \times M$ resistors of resistivity R_0, confirming that it is equivalent to M parallel resistors, each of value $N \times R_0$. If, for example, $N \times M = 291 \times 190$ resistors with $R_0 = 1\ \text{k}\Omega$ are considered, the total resistance of the net resulted exactly $1 \times 291/190 = 1.53\ \text{k}\Omega$. Nanowire failures, due to defects in the fabrication process, have been modeled by randomly removing resistors from the net, as schematically shown in Fig. 3d. For each resistor, a random number with a uniform distribution between 0 and 1 has been generated [13] and compared with a threshold P that established the probability (percentage) of failures: the resistor is removed if the random number is below the threshold P. The random removal of resistors has been repeated a suitable number (n) of times (population), starting from the same initial resistor network, and the total resistance of each remaining random network has been evaluated. For each percentage of removed resistors, the average value of the total resistance has been evaluated

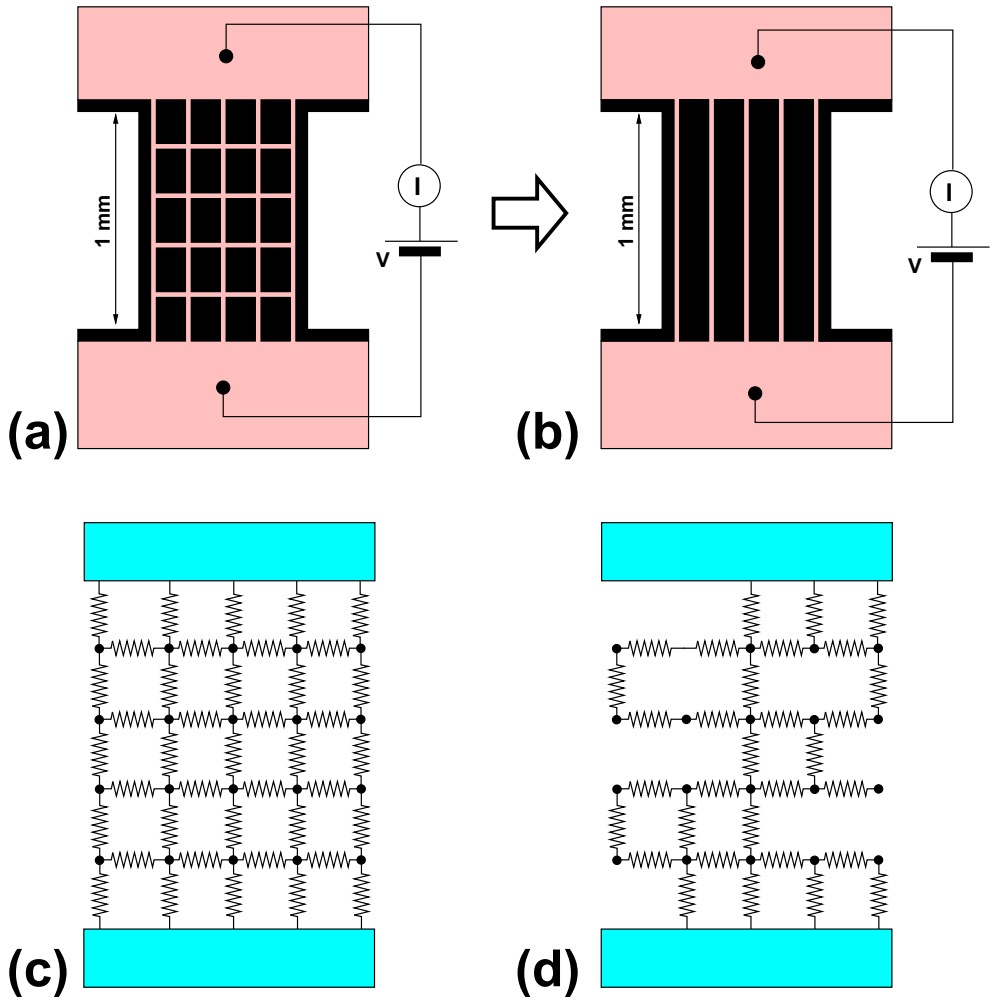

Fig. 3. Sketch of a SiNW network (a), electrically and thermally equivalent to many very long SiNWs in parallel (b). In (c) the equivalent electrical resistor network is shown and in (d) it is shown how random nanowire failures can be modeled by removing resistors from the net.

in the population n. Fig. 4a shows the average resistance ($n = 100$) of a network with an initial number of resistors $N \times M$ 291 × 190, each with a resistance of 33 kΩ, as a function of percentage of failure (i.e. percentage of randomly removed resistors). It can be seen that the average resistance value shows a reduced variation even up to high percentages of failure. For example, the resistance increases from 51 kΩ (no failures) to 63 kΩ in the case of 10% of failures. According to the bond percolation theory [14,15], a full failure (disconnection between top and bottom contacts) occurs only for very high nanowire failure percentages; in the case of Fig. 4a, only failure percentages greater than 50% gives a complete disconnection between the top and the bottom contacts of the network.

In the case of M parallel resistors, each representing a millimeter long nanowire (no horizontal branches), the reliability of the top to down connection with respect to nanowire failure is much smaller. The same defect density can be modeled by considering each long nanowire as the series of N elementary resistors R_0 (conductivity G_0) identical to those forming the network, and marked by the same failure probability P. The failure of a single elementary resistor of the series leads to the failure of the entire long nanowire. The probability that an elementary resistor R_0 does not fail is $1 - P$; making the reasonable hypothesis that failure events are uncorrelated, the probability that the series (the sum) of N resistors does not fail is the product of each single probability. Therefore the probability of conduction for a millimeter long nanowire is $(1 - P)^N$. This probability results to be very small even with low P since N is of the order of several hundreds. If M long nanowires are placed in parallel, the total conductance can be evaluated as $G = M \times G_0/N$ in the case of no failures (no defects); in the case of failures with probability P, the expression for the total conductance can be evaluated as $G = M \times G_0 \frac{(1-P)^N}{N}$. For example, by considering again $R_0 = 33$ kΩ, ($G_0 = 3.03 \times 10^{-5}\ \Omega^{-1}$), the total conductance in the case of 10% of failures ($P = 0.1$) is $G = 3.16 \times 10^{-14}\ \Omega^{-1}$ and the total resistance is $1/G = 3.17 \times 10^{13}\ \Omega$, i.e. top and bottom are practically disconnected.

Tolerance of the total net electrical resistance with respect to nanowire width dispersion has been investigated. Random resistance networks have been generated by randomly varying the width of the single wires and evaluating the resistance by considering an ohmic behavior for the latter. Each nanowire has a length of 3 μm and a random width generated by means of a gaussian random generator [13] with a given average width of 80 nm and standard deviation σ. Fig. 4b shows the average total network resistance, evaluated on 100 random nets (generated by different seeds), as a function of the nanowire width standard deviation σ. The errorbars show the standard deviations of the total net resistance, that resulted to be very small if compared to the relatively high dispersion of the nanowire width. For example, given a

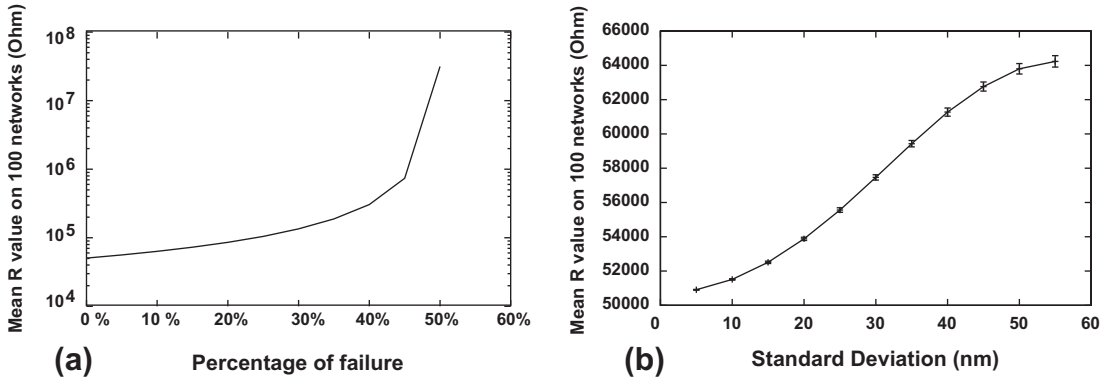

Fig. 4. In (a) the average value of resistance, evaluated on 100 networks with 291 × 190 initial number of resistors, is reported as a function of percentage of randomly removed resistors, that simulated the nanowire failure. In (b) the average value of resistance, evaluated on 100 networks with 291 × 190 random resistors, is reported as a function of the silicon nanowire width dispersion (standard deviation).

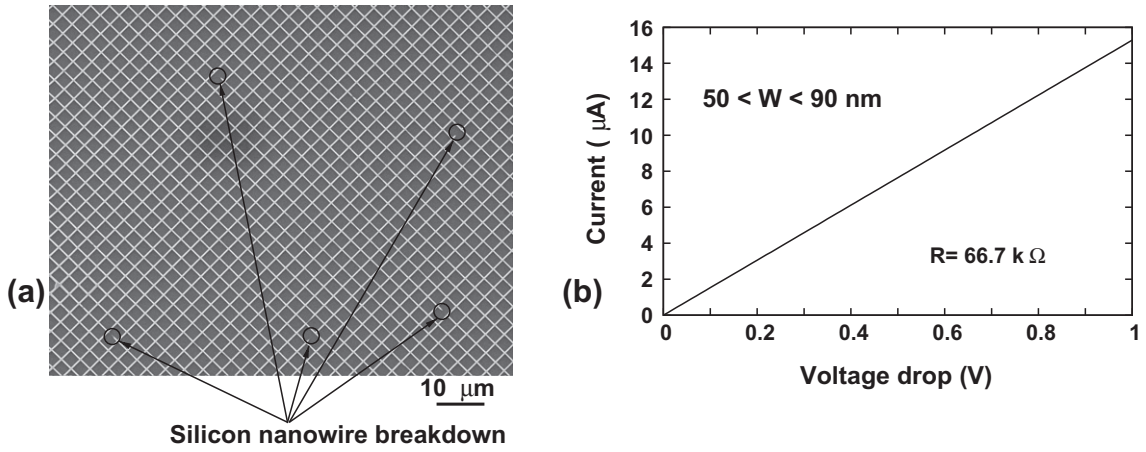

Fig. 5. In (a) a SEM image of a portion of SiNW network is shown; nanowire failures are enlightened. In (b) the *I–V* characteristics of the SiNW network shown in (a), measured between the top and bottom contacts, is reported. The conduction is linear and the resistance is very similar to the one of many small and long silicon nanowires.

σ = ±50 nm (more than 60% of the average width of 80 nm), the total average resistance is 63801 Ω with a standard deviation of ±303 Ω that is less than 5%. This demonstrates the robustness of the total electrical resistance of the net with respect to the nanowire width dispersion.

4. Network reliability and electrical characterization

An estimation of nanowire failure percentage in fabricated networks, as the one shown in Fig. 1, can be performed by means of SEM inspection. For example, SEM photo of Fig. 5a shows a portion of a typical SiNW network, and interruptions (broken nanowires) in the network are enlightened. By inspecting several samples of fabricated SiNW networks, we can conclude that the mean value of failures is between 10% and 15%. This value is well below the threshold failure percentage for which the whole resistance grows up noticeably. An estimation of the dispersion of SiNW width *W* has been also performed by SEM inspection and in a very large portion of the device it resulted between 50 and 90 nm. Fig. 5b shows a typical *I–V* characteristic measured for a SiNW network. The ohmic behavior shows that nonlinear effects in the conduction are negligible, and the value of about 66.7 kΩ is consistent to the above considerations about the electrical equivalence of the whole network with a large number of 1 mm long single nanowires in parallel. Indeed, from previous electrical measurements of a single SiNW, the conductivity can be estimated to be $40 \times 10^3\ \Omega^{-1}\,m^{-1}$ (heavily doped wires). The measured resistance value of the network is comparable to the one of 190 SiNWs in parallel, with a length of 1 mm and a width mean value $W \simeq 72$ nm, which is very close to the *W* mean value observed by SEM inspection in a very large region of the device. Moreover, as it has been previously demonstrated, even a large dispersion in the width at the boundaries of the device, does not affect the electrical characteristics of the network significantly, since the whole behavior of such devices is dominated by the large number of SiNWs smaller than 90 nm observed inside the structure.

These results are very promising for the fabrication of large area silicon nanowire networks that could allow practical applications of the interesting properties of SiNWs. In particular, the equivalence of reliable networks to the parallel of many, millimeters long, SiNWs makes this technique suitable for the fabrication of high efficiency thermoelectric devices. The possible implementation of this technique with advanced optical lithography is very promising for the fabrication of even larger areas SiNW networks to be applied to energy harvesting.

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